

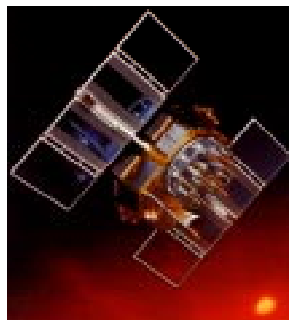


## User Guide

CG1-RADIO • ***CompactPCI***<sup>®</sup> GPS Receiver

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## About this Manual

This manual describes some technical aspects of the CG1-RADIO, required for installation and system integration. It is intended for the experienced user only.

### Edition History

EKF Document	Ed.	Contents/ <i>Changes</i>	Author	Date
Text # 2460 cg1uge.wpd	1	1. Edition User Manual CG1-RADIO English Language Document Preliminary edition, to be completed later on	jj	25 May 2001

### Nomenclature

Signal names used herein with an attached '#' designate active low lines.

### Trade Marks

Some terms used herein are property of their respective owners, e.g.

Pentium, Celeron, Socket 370: ® Intel

***CompactPCI***: ® PICMG

Windows 98, Windows NT, Windows 2000: ® Microsoft

EKF does not claim this list to be complete.

### Legal Disclaimer - Liability Exclusion

This manual has been edited as carefully as possible. We apologize for any potential mistake. Information provided herein is designated exclusively to the proficient user (system integrator, engineer). EKF can accept no responsibility for any potential damage caused by the use of this manual.

## CG1-RADIO Features

## Feature Summary

<b>Printed Circuit Board</b>	<b>Dimensions</b>	3U Eurocard (100x160mm <sup>2</sup> ), front panel width 20.3mm (4HP), mechanics constructed with respect to EMC requirements, ejector lever
<b>CPU</b>	<b>Microprocessor</b>	Intel i960RP/RD, 3.3V, 33/66MHz, clocked by system bus (local oscillator provided when operated as stand-alone)
	<b>Memory</b>	4MBytes FPM/EDO DRAM, 32-bit, 4MBytes FLASH ROM (SMT) 28F160S5 (Intel, Sharp), 32-bit
	<b>Utilities</b>	Watchdog and 5V/3.3V voltage-supervisor MAX705, serial EEPROM 4KByte I <sup>2</sup> C, optional: ACCESS.bus interface
	<b>Firmware</b>	Mon960 Monitor/Debugger
<b>Serial Interfaces SP1 (internally) and SP2 (externally and internally)</b>	<b>Protocol</b>	Asynchronous, serial protocol: 1 startbit; 7 or 8 databits; 1 or 2 stopbits; optional even/odd parity; standard bitrates up to 115,2 kbps, default parameters for GPS operation SP1=4800Baud (GPS NMEA-0183), SP2=9600Baud (DGPS RTCM SC-104)
	<b>Serial Interface Controller</b>	2 x 16C550 asynchronous communication element, e.g. Texas Instruments TL16C550C or equivalent
	<b>Physical Interface SP2</b>	RS-232E/V.28, PC compatible D-SUB connector male 9-pin, to be used either as DGPS input or as universal serial COM port, ESD protection 10kV, pin 9 configurable either as RS-232 RI input or +12V power supply output to external DGPS receiver (PolySwitch resettable fuse 100mA)
	<b>Drivers</b>	Serial drivers (COM port emulation) available for Windows NT4.0 and Windows 2000, others forthcoming
<b>GPS</b>	<b>Receiver Module</b>	Exchangeable modular 12-channel receiver, chip set Conexant (Rockwell) Zodiac, SMB jack for 1575,42MHz (L1 Band) GPS antenna active or passive, RF signal level at 130dBW ... - 163dBW, antenna supply 0V, +5V, +12V selectable with jumper JANT (PolySwitch resettable fuse 100mA)
	<b>Data Retention Warmstart</b>	Keep-Alive power condition for enhanced TTFF upon power-up (Time To First Fix), SRAM and RTC data non-volatile buffered by Lithium cell 190mAh (>4500h)
	<b>Software</b>	NMEA protocol based application programs
<b>CompactPCI<sup>®</sup> Bus</b>	<b>Connector J1</b>	32-bit, 33MHz (133MB/s) DMA bus master 5V interface
<b>Power Supply</b>	<b>Connector J1</b>	+5V ±5% 0.5A max. +3.3V ±0,3V 0.7A (i960RP) 0.9A (i960RD) max. +12V ±5% 0.1A max. -12V ±5% 0.1A max.
<b>Temperature Humidity</b>	<b>Operating</b>	operating temperature 0-70°C humidity 5-90% non condensing

## Short Description

*Both, the global time (UTC) and the geographic position, provides the **CompactPCI®** based GPS receiver board **CG1-RADIO** manufactured by EKF.*

Most industrial computer systems need synchronization to a precise time standard. A solution to this problem would be any radio controlled clock. Unfortunately, most countries have their own local transmitter standards (if any). Hence, for universal use (e.g. if systems are mobile or destined for export), a GPS based clock is the best choice.

The **Global Positioning System** provides the **Universal Time (Coordinated)** and - of course - position data. Most useful for mobile applications, also country specific program versions could be executed automatically. A CG1-RADIO equipped system can signal its current position to a remote computer.

The CG1-RADIO module is housed on a single size Eurocard (3U). The board is provided with a high performance 12 parallel-channel receiver engine continuously tracking all satellites in view, thus providing accurate positioning and time data. The receiver is compatible with passive or active antennas and supports the NMEA-0183 data protocol.

Direct, differential RTCM SC-104 data capability dramatically improves the positioning accuracy. For that, the CG1-RADIO is equipped with a serial port for communication with an external DGPS receiver.

From the hosts view, the enclosed drivers reduce the CG1-RADIO board to one or two common serial ports, e.g. COM3/4. Therefore all programs based on the NMEA-0183 data protocol can be executed without modification.



The highly integrated digital GPS receiver uses the Zodiac chip set (Rockwell/Conexant) and is accommodated on a miniature daughter board as an exchangeable sub-assembly. The 12-channel architecture provides rapid Time-To-First-Fix (TTFF) under all startup conditions. The receiver decodes and processes signals from all visible GPS satellites, thereby producing a highly accurate and robust navigation solution. The external GPS antenna connects to the front panel mounted SMB style jack and must have reasonable visibility of the sky. For best performance, use an active antenna, especially for a cable length of 3m and above.

Due to Selective Availability (SA) the GPS navigation accuracy is limited to 100m for civil use. The CG1-RADIO however as an option allows to read in an external differential signal (DGPS) in order to reduce the positioning error to 3-5m. For this, the CG1 is provided with a 9-pin D-SUB connector (front panel) serial interface port. Incoming DGPS data must conform to the international RTCM SC-104 protocol. The type of the external DGPS receiver depends on the location. In Germany e.g. there is a choice between the LW ALF transmitter (Mainflingen, Deutsche Telekom) or the RASANT FM RDS System (ARD).

Equipped with the powerful embedded processor i960RP(D), the board profits from the built-in PCI bridge as interface to the **CompactPCI®** system bus. For typical applications, the EKF software drivers let the CPCI system host view the CG1-RADIO module as 16C550 UART based dual serial adapter card.

The first serial port of the CG1-RADIO is for on-board use only. It serves as a communications interface to the GPS receiver. Commands and data can be sent to and received from the GPS daughter board according to the NMEA-0183 standard protocol. The moderate transmission rate of 4800bps cares for low interrupt load of the system host.

The second serial port is intended either as external DGPS interface (read only), or as a general purpose RS-232E communications channel. The wiring of the front panel mounted 9-pin male D-SUB connector SP2 is identical to desktop PC COM ports. When receiving differential DGPS data at 9600bps according to the RTCM SC-104 standard, the GPS daughter module uses this information for its internal calculations to sharpen the positioning data. The second serial interface is also directly readable by the system host. Programs as LabMon (Rockwell/Conexant) need DGPS data in parallel to the GPS receiver for presentation.

If the DGPS data capability of the CG1-RADIO is not used, then the serial port SP2 is available for general purpose I/O applications.

The EKF drivers treat the CG1-RADIO module as 16C550 compatible COM ports. While the drivers allow arbitrary names e.g. COM16, practically there exist limitations in most systems. Typically, COM1 and COM2 are reserved names for the host CPU's serial interfaces. On the other hand, most GPS and communications applications will support COM1..4 only. Therefore COM3 is recommended to control the GPS NMEA port (first serial interface of the CG1-RADIO), and COM4 to be used as DGPS RTCM receiver (second serial port, SP2).

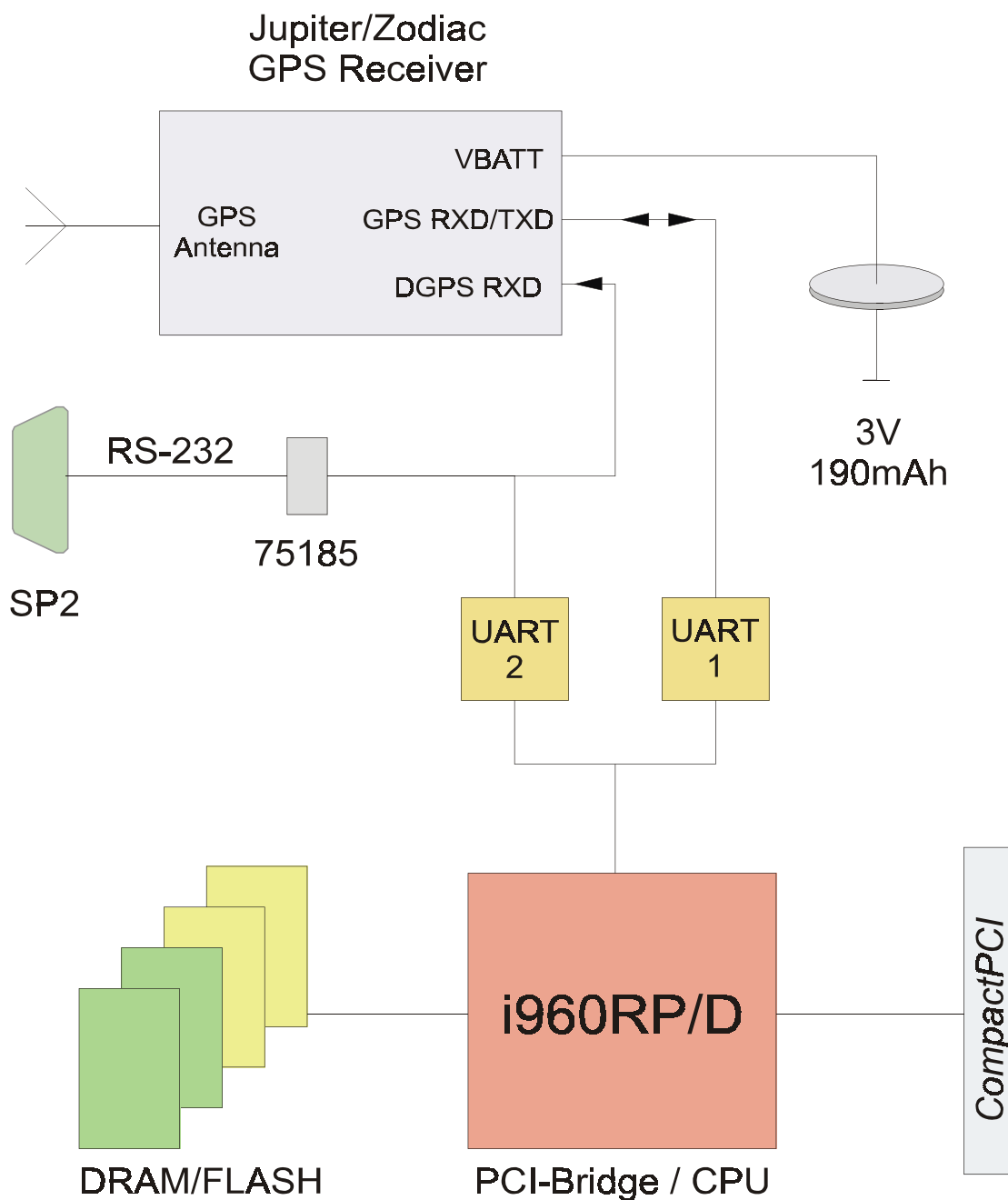
There are many commercial GPS application programs available, often allowing cartographical visualization. In addition, the Internet is full of GPS shareware tools. The common basis of most applications is the NMEA-0183 protocol, so that they should be usable with the CG1-RADIO without any modification.

Developers might prefer to sample and compute GPS data locally on the CG1 board. This can be achieved by the local i960 processor. Program and data can be stored in a generous amount of local memory (4MB DRAM and 4MB Flash EEPROM). As a development tool, EKF provides the resident monitor/debugger MON960, which allows stand-alone operation and download of programs via CPCI bus or serial interface SP2. Furthermore EKF can offer turn key ready application programming support.

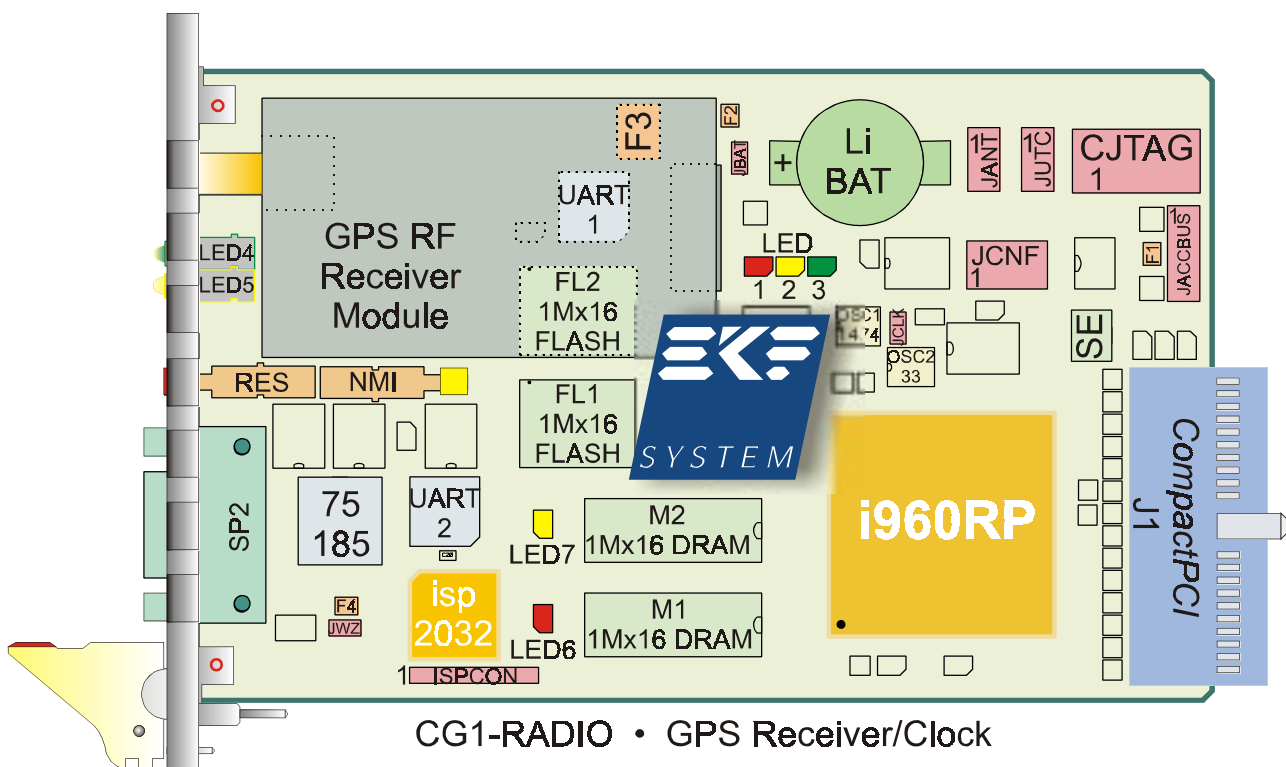
The CG1-RADIO module lends full GPS functionality to any industrial **CompactPCI®** system. Beginning with applications needing absolute time stamps or isochronous control of tasks, up to programs requiring three-dimensional navigation, the CG1-RADIO board is the perfect and affordable choice wherever GPS can solve a problem.



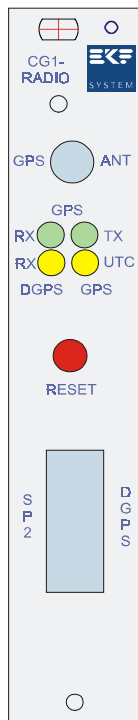
Block Diagram



Top View Component Assembly



Front Panel



## Front Panel Elements

ANT	RF input 1575,42MHz (L1 band), GPS antenna active or passive, input signal level at -130dBW ... -163dBW, SMB jack, power supply voltages selectable 0V, +5V, +12V (jumper JANT), PolySwitch resettable fuse 100mA
SP2	RS-232E D-SUB 9 male connector, can be used either as universal serial COM-port (standard bitrates up to max. 115,2 kBaud), or as DGPS input (according to RTCM SC-104 protocol, 9600bps, 8bit, 1 startbit, 1 stopbit, no parity)
LED Array	RXD/TXD GPS receiver module RXD serial port SP2 UTC pulse 1s period
RES	Push button switch Reset (local CPU)

## Strapping Headers

JANT	Antenna passive, antenna active +5V, antenna active +12V
JBAT	Lithium battery for data retention of GPS module's RTC and SRAM
JCLK	CPU clock derived locally or from CPCI bus
JCNF	CPU behaviour after reset, effects of CPCI reset on CG1-RADIO
JWZ	Serial port SP2 D-SUB pin 9, configured either as RS-232 RI input or +12V output as power supply to external WZ DGPS receiver

## Connectors &amp; Sockets

CJTAG	JTAG testport
ISPCON	ispGAL programming port
JACCBUS	I <sup>2</sup> C-Bus expansion interface
JUTC	TTL time mark pulse 1Hz and 10kHz, synchronized to the UTC Universal Time (Coordinated)

## Installation

### Before You Begin

### Warnings

The procedures in this chapter assume familiarity with the general terminology associated with industrial electronics and with safety practices and regulatory compliance required for using and modifying electronic equipment. Disconnect the system from its power source and from any telecommunication links, networks or modems before performing any of the procedures described in this chapter. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage. Some parts of the system can continue to operate even though the power switch is in its off state.



### Caution

Electrostatic discharge (ESD) can damage components. Perform the procedures described in this chapter only at an ESD workstation. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis or board front panel. Store the board only in its original ESD protected packaging. Retain the original packaging (antistatic bag and antistatic box) in case of returning the board to EKF for repair.




## Installing the Board

### Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

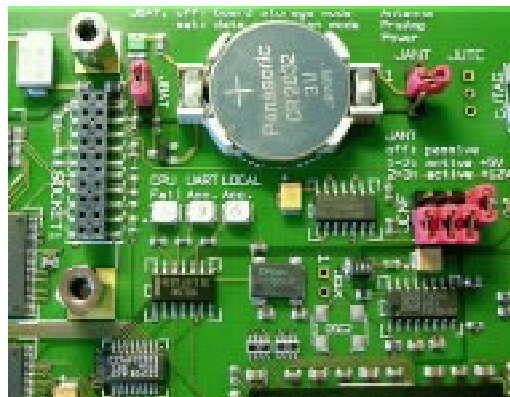
Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system 
- Remove the board packaging, be sure to touch the board only at the front panel
- Configure any jumpers on the board according to your application (see next page 'Jumper Configuration')
- Identify the related CompactPCI slot (peripheral slot for I/O boards)
- Insert card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighbored front panels)
- A card with on board connectors requires attachment of associated cabling now
- Lock the ejector lever, fix screws at the front panel (top/bottom)
- Retain original packaging in case of return

## Jumper Configuration & Factory Defaults

Before inserting the CG1-RADIO into your CPCI enclosure, please control the settings of some jumper fields on the board. Typically, there are two jumpers that need adjustment.

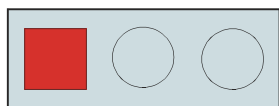
- Set the jumper JBAT. This enables the Lithium cell, which provides for saving satellite tracking information in a buffered SRAM, and supplies the RTC, which is operating as clock source while the system is powered down or there is no receiver signal available on the antenna input.
- Check the jumper JANT according to the antenna in use. If your antenna is equipped with a cable more than 2m length, probably it has a built-in amplifier (active antenna). If you cannot determine the type of antenna, try the passive mode first (JANT open). Observe the front panel LED UTC, which sends a periodic signal when the receiver gets valid GPS data (there may be some delay time). If this procedure is not successful, set the JANT jumper to the +5V active antenna mode. Note: GPS antennas need free sky above them (mounting outside the building required).



Jumper JANT, JBAT, JCNF

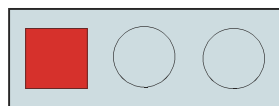
These jumpers are located near the Lithium cell

## JANT



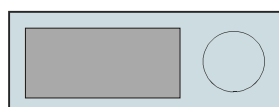
- 1 +5V  
2 Antenna PreAmp Power  
3 +12V

Check your antenna type in use! If in doubt, use default configuration (no antenna power - passive antenna).



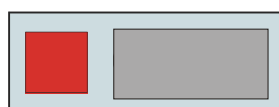
- 1  
2  
3  
passive antenna (default)

Use this configuration if in doubt (passive antenna, JANT left open)



- 1 2 3  
active antenna +5V

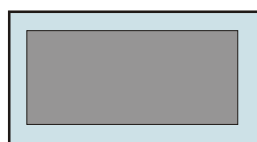
This configuration is typical for active antennas (set to +5V power source, JANT 1-2 closed)



- 1 2 3  
active antenna +12V

Seldomly used +12V active antenna - warning: you could possibly damage +5V antennas if set to +12V

## JBAT



- 1 2  
GPS RTC & SRAM  
data retention mode

JBAT provides for non-volatile GPS RTC & SRAM data (Lithium cell)

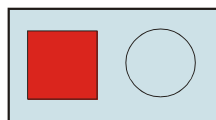
jumper 1-2 open - saves cell lifetime while board storage (delivery status)

**jumper 1-2 closed - data retention mode**

factory default is off - check this setting if TTFF is slow

you have to set this jumper on a new board - EKF opens this jumper for storing and shipping

## JCLK



1 2

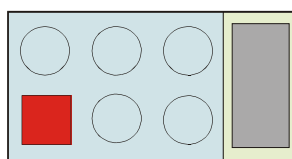
Default:  
Open (Bus Clock)

Clock Source Selector:

Local clock sourced from *CompactPCI*® Bus Clock  
(this jumper is normally not stuffed)

## JCNF

default configuration



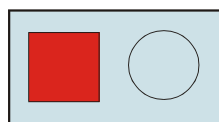
1 2 3 4

Open 1 2 3  
Closed 4

i960®RP Configuration Selector:

1. Initialization mode 3 (CPU starts after reset)
2. Retry CPCI configuration cycles
3. BIST active
4. **CPCI reset passed through to local reset**

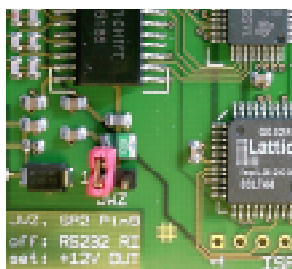
## JWZ



1 2

JWZ allows for passing +12V power on the RI pin of SP2 in order to supply an external DGPS receiver, which can sharpen the GPS positioning information when the Selective Availability feature of the GPS system is activated.

**JWZ default mode is jumper off**



Jumper JWZ


JWZ can be found near the front panel ejector lever

## Removing the Board

### Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system 
- Identify the board, be sure to touch the board only at the front panel
- unfasten both front panel screws (top/bottom), unlock the ejector lever
- Remove any onboard cabling assembly
- Activate the ejector lever
- Remove the card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighbored front panels)
- Store board in the original packaging, do not touch any components, hold the board at the front panel only

### Warning

Do not expose the card to fire. Battery cells and other components could explode and cause personal injury.



## EMC Recommendations



In order to comply with the CE regulations for EMC, it is mandatory to observe the following rules:

- The chassis or rack including other boards in use must comply entirely with CE
- Close all board slots not in use with a blind front panel
- Front panels must be fastened by built-in screws
- Cover any unused front panel mounted connector with a shielding cap
- External communications cable assemblies must be shielded (shield connected only at one end of the cable)
- Use ferrite beads for cabling wherever appropriate
- Some connectors may require additional isolating parts (e.g. 10Base-2 BNC T-connector)

## Reccomended Accessories

Blind CPCI Front Panels	EKF Elektronik	Widths currently available (1HP=5.08mm): with handle 4HP/8HP without handle 2HP/4HP/8HP/10HP/12HP
Ferrit Bead Filters	ARP Datacom, 63115 Dietzenbach	Ordering No. 102 820 (cable diameter 6.5mm) 102 821 (cable diameter 10.0mm) 102 822 (cable diameter 13.0mm)
Isolating Elements	ARP Datacom, 63115 Dietzenbach	Ordering No. 182 068 (Cheapernet T-connector)
Metal Shielding Caps	Conec-Polytronic, 59557 Lippstadt	Ordering No. CDFA 09 165 X 13129 X (DB9) CDSFA 15 165 X 12979 X (DB15) CDSFA 25 165 X 12989 X (DB25)

## Replacement of the Battery

When your system is turned off, a battery maintains the current time-of-day clock and the values in the GPS receiver modules CMOS RAM current. The battery allows for nominal 4750hrs data retention. For replacement, the old battery must be removed from its socket. Change it against the same type only (Panasonic CR2032 3V). Observe the cell polarization - the '+' mark appears on top.

*Be very careful when removing the battery from its socket. Do not damage any components or copper traces situated under the battery holder.*

## Warning

Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type. Do not expose a battery to fire.



## Technical Reference

### GPS Receiver Module

#### General Features

The CG1-RADIO is equipped with the Conexant Jupiter GPS receiver module, a 12 parallel channel receiver engine. Each of these receivers continuously tracks all satellites in view and provides accurate satellite positioning data. The highly integrated digital receivers incorporate two custom Conexant devices including the Conexant Zodiac chip set: the "Gemini/Pisces" MonoPac™ and the "Scorpio" Digital Signal Processor (DSP). The combination of custom devices minimizes the module size to about 28 square centimeters and satisfies harsh industrial requirements. The Jupiter module decodes and processes signals from all visible GPS satellites. These satellites, in various orbits around the Earth, broadcast radio frequency (RF) ranging codes and navigation data messages. The Jupiter receiver uses all available signals to produce a highly accurate and robust navigation solution.

The 12-channel architecture provides rapid Time-To-First-Fix (TTFF) under all startup conditions. While the best TTFF performance is achieved when time of day and current position estimates are provided to the receiver, the flexible Zodiac signal acquisition system takes advantage of all available information to provide a rapid TTFF. Acquisition is guaranteed under all initialization conditions as long as visible satellites are not obscured. To minimize TTFF following a power down, the Jupiter receiver is sourced by a Lithium Cell on the CG1-RADIO board to maintain power to the Static Random-Access Memory (SRAM) and Real-Time Clock (RTC) for periods following the loss of prime power. The use of the battery voltage assures the shortest possible TTFF following a short power down. The Jupiter receiver supports two dimensional (2-D) operation when less than four satellites are available or when required by operating conditions. Altitude information required for 2-D operation is determined by the receiver.

The Jupiter module contains two independent serial ports, one of which is configured for primary input and output data flow using the National Marine Electronics Association (NMEA-0183) format or Conexant binary message format. The second port is used to receive Differential GPS (DGPS) corrections in the Radio Technical Commission For Maritime Services (RTCM SC-104) format. The Jupiter receiver supports DGPS operations for dramatically improved accuracies over standard GPS (while Selective Availability is activated by US government). The modules primary I/O port (NMEA) is connected to the UART1 of the CG1-RADIO, while the secondary port (RTCM) is connected to both the front panel connector SP2 and the UART2 of the CG1-RADIO (see block diagram CG1-RADIO).

For applications that require timing synchronization to GPS accuracies, the Jupiter receiver provides an output timing pulse that is synchronized to one second Universal Time Coordinated (UTC) boundaries. This timing pulse is available by an optional single row header JUTC on the CG1-RADIO board, and it is also used to drive an indicator LED visible from the CG1-RADIO boards front panel.

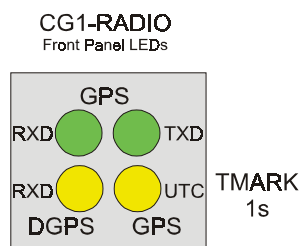
## Serial Ports & Protocols

The Jupiter module communicates with the host across its primary serial port. The bit rate is fixed to 4800bps, no parity, 8 data bits, 1 stop bit. Commands are passed to the module, which responds accordingly with results and status information. Due to the low data transfer rates, there is no hardwired handshake available.

There are two choices for protocol selection. By default, the NMEA standard is selected on the Jupiter Module. This is an ASCII based protocol, widely accepted as a common base to all GPS application programs. As an alternate, the Jupiter module can be configured to communicate by a proprietary, binary protocol (Rockwell/Conexant). On writing own firmware, the binary protocol could be a more efficient solution. The binary protocol also allows for defining higher bit rates on both serial interfaces. Please contact EKF when you need the binary protocol feature.

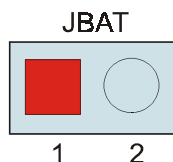
The secondary (auxiliary) serial port of the Jupiter module is configured as a half duplex input at 9600bps, no parity, 8 data bits, one stop bit. This interface is configured to receive RTCM DGPS correction data messages. Usage of this port is optional.

There are indicator LEDs mounted in the front panel to signal both RXD and TXD of the primary serial interface, and RXD only of the auxiliary serial interface.



## Auxiliary Power

The CG1-RADIO is equipped with a Lithium cell battery. Close the jumper JBAT to provide this auxiliary power to the Jupiter receiver module (you have to set this jumper for any new board, because the factory default is off for saving cell lifetime while storing). Data retention for the GPS receivers SRAM and RTC is nominal 4750hrs. Loss of SRAM or RTC data results in slower response time (TTFB) after powering up the CG1-RADIO, but the GPS receiver remains fully operable. For replacement of the battery, observe precautions and follow the procedure described in chapter 'Replacement of the Battery'.

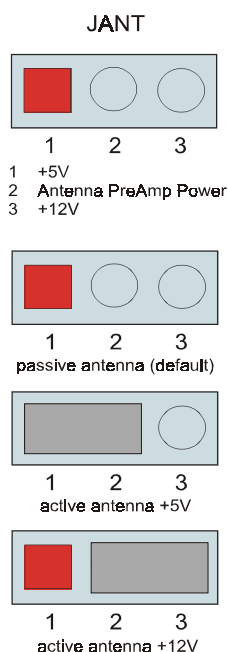


JBAT provides for non-volatile  
GPS RTC & SRAM data  
jumper off - saves cell lifetime while board storage  
jumper set - data retention mode  
  
factory default is off -  
check setting if TTFB is slow

## Antenna Connector

The Jupiter receiver is equipped with a SMB type miniature coaxial female connector as RF signal input from the antenna. The antenna cable therefore should provide a matching SMB plug. When ordering an antenna, be sure to have selected the SMB connector version, if the antenna cable is directly attached (there are several other common connector types on the market, e.g. SMA, TNC and OSX). If the antenna is equipped with a built-in connector, an additional adapter cable is required, matching both, the antenna type of connector at the outer end, and a SMB male connector on the CG1-RADIO side. The SMB connector should be a straight type, not right angle style. A right angle connector might have a profile too low to allow full insertion into the matching jack on the CG1-RADIO, which is mounted behind the front panel, due to EMC requirements.

For best results, use an active GPS antenna with built-in amplifier, especially when the cable length exceeds 2m. Typical gain is 10...50db; a longer cable needs higher gain to compensate its loss. Active antennas are powered by +5V or +12V across the coaxial cable, selected by the jumper field JANT. Do not obscure the antenna (mounting outside of the building required).



**WARNING:** unmatched JANT settings may destroy antenna  
check setting anytime before connecting GPS antenna



Heavy Duty Airborne GPS Antenna

## Jupiter Module Socket

The Jupiter receiver module fits into a dual row, 20-position, 2.0mm metric socket and is mechanically fixed by 4 screws .

		Socket1			
+5V <sup>1</sup>	1	2	+5V/+12V Antenna <sup>2</sup>		
	3	4	VBATT		
	5	6	RESET#		
GPIO3 <sup>4</sup>	7	8	GPIO2 <sup>4</sup>		
GND	9	10			
Serial Data In 1	11	12	Serial Data Out 1		
	13	14	GND		
GND	15	16	Serial Data In 2 <sup>3</sup>		
GND	17	18	GND		
UTC 10kHz	19	20	UTC TMARK		

<sup>1</sup> Jupiter receiver power, fused by PolySwitch 0.3A

<sup>2</sup> Antenna power, from JANT, selectable NC/5V/12V, fused by PolySwitch 0.1A

<sup>3</sup> RTCM DGPS optional input, can be fully deactivated by removing R36 and placing R37

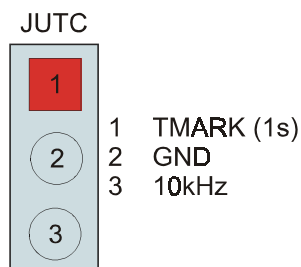
<sup>4</sup> GPIO2/3 inputs are used to setup some Jupiter options, see table below

GPIO2	Resistor Stuffed	Jupiter Option
0	R29 stuffed R28 removed	NMEA 4800bps ASCII protocol, no parity, 1 start bit, 8 data bits, 1 stop bit, default
1	R28 stuffed R29 removed	Protocol either Conexant binary, 9600bps, 1 start bit, 8 data bits, 1 stop bit, or as defined in Jupiter non-volatile memory, depends on how GPIO3 is configured

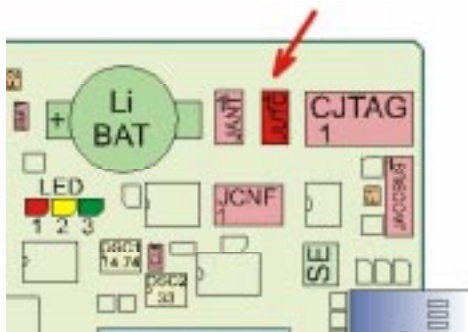
GPIO3	Resistor Stuffed	Jupiter Option
0	R33 stuffed R32 removed	Jupiter receiver gets its initializing parameters from its ROM
1	R32 stuffed R33 removed	Jupiter tries to read initializing parameters from its SRAM first (if valid), else from its EEPROM (if valid), else falls back to its ROM stored parameters, default

## Jumper JUTC, Time Mark

The CG1-RADIO can be used to synchronize external events with the UTC (Universal Time Coordinated). The board generates two output signals, named **utctmark** and **utc10kHz**, which can be used for various purposes. Both signals are wired to the (optional) 3-pin header connector JUTC.



This connector is located near the Lithium cell. If the board is not equipped with this (optional) connector, the position can easily be filled by the customer with a three pin 0.1" (2.54mm) pitch header.



The Time Mark output **utctmark** provides a one pulse-per-second (1pps) signal to the user specific application. When the receiver provides a valid navigation solution, the rising edge of each utctmark pulse is synchronized with the UTC one second epochs to within  $\pm 300\text{ns}$ . This signal is a positive logic, buffered CMOS level output pulse that transitions from a logic 'low' condition to a logic 'high' at a 1 Hz rate. The pulse duration is typically 25.6ms. The 10kHz UTC Synchronized Clock signal **utc10kHz** is a symmetric, buffered CMOS level output, synchronized to the utctmark pulse.

## Additional Documentation

In addition to this manual, EKF provides detailed on-line information regarding the Jupiter receiver module (PDF documents). Also use the Conexant homepage for most recent information:

<http://www.conexant.com>

Document Title	URL http://
<i>Jupiter GPS Receiver Data Sheet</i>	<a href="http://www.ekf.de/c/cgps/cg1/info/jupiter.pdf">www.ekf.de/c/cgps/cg1/info/jupiter.pdf</a>
<i>GPS Receiver Designers Guide</i>	<a href="http://www.ekf.de/c/cgps/cg1/info/designerguide.pdf">www.ekf.de/c/cgps/cg1/info/designerguide.pdf</a>
<i>Serial Data Interface Specification</i>	<a href="http://www.ekf.de/c/cgps/cg1/info/iospec_r11.pdf">www.ekf.de/c/cgps/cg1/info/iospec_r11.pdf</a>
pointers to some other documentation	<a href="http://www.ekf.de/c/cgps/cg1/cg1.html">www.ekf.de/c/cgps/cg1/cg1.html</a>

The NMEA and RTCM protocol specifications can be obtained from

<http://www.nmea.org/0183.htm>

<http://www.rtcn.org/>

## Microprocessor

### General Features

The central unit on the CG1-RADIO is an i960<sup>®</sup>RP I/O Processor, a member of the 80960 family of high performance processors. It combines a high-speed CPU with powerful features to create an intelligent I/O processor and integrates it into a Peripheral Components Interconnect (PCI) environment. This multi-function PCI device is fully compliant with the *PCI Local Bus Specification*, revision 2.1. The i960<sup>®</sup>RP local bus, a 32-bit multiplexed burst bus, is a high-speed interface to system memory and I/O. Physical and logical memory attributes are programmed via memory-mapped control registers (MMRs). The core can maintain a sustained execution rate of one instruction per clock of most instructions.

The i960<sup>®</sup>RP features include:

- Single-clock execution of most instructions
- Independent Multiply/Divide Unit
- 128-bit register bus speeds local register caching
- 4 Kbyte two-way, integrated instruction cache
- 2 Kbyte direct-mapped, integrated data cache
- 1 Kbyte integrated, zero wait state data RAM
- PCI-to-PCI Bridge Unit
- Address Translation Unit
- DMA Controller
- Messaging Unit
- Memory Controller
- I<sup>2</sup>C Bus Interface Unit

The Address Translation Unit (ATU) permits direct data access from the **CompactPCI**<sup>®</sup> interface to local memory. This allows for example the programming of the FLASH devices or downloading software to local memory via the primary **CompactPCI**<sup>®</sup> interface without interaction of the i960<sup>®</sup>RP core. Address translation is controlled through programmable, memory-mapped registers accessible from both the PCI interface and the i960 core processor. The primary ATU has a dedicated PCI configuration space that is accessible through the **CompactPCI**<sup>®</sup> bus or the i960 core.

The DMA Controller allows low-latency, high-throughput data transfers between PCI bus agents and i960<sup>®</sup>RP local memory. Three separate DMA channels accommodate data transfers: two for the **CompactPCI**<sup>®</sup> bus, one for the secondary PCI bus (not usable on the CG1-RADIO). The DMA Controller supports chaining and unaligned data transfers.

The Messaging Unit (MU) provides data transfer between the PCI system and the i960<sup>®</sup>RP. It uses interrupts to notify each system when new data arrives. The MU has four messaging mechanisms: Message Registers, Doorbell Registers, Circular Queues and Index Registers. Each allows a host processor or external PCI device and the i960<sup>®</sup>RP to communicate through message passing and interrupt generation. The MU makes it easy to realize the Intelligent I/O Interface I<sub>2</sub>O.

The Memory Controller allows direct control of the external memory respectively the memory-mapped I/Os on the CG1-RADIO, including DRAM and Flash EEPROM. It features programmable chip selects and a wait state generator. External memory can be configured as PCI addressable memory or private i960<sup>®</sup>RP memory.

Since there is no need for it, the secondary PCI interface of the i960<sup>®</sup>RP is unconnected on the CG1-RADIO. Therefore neither the PCI-to-PCI Bridge unit nor the secondary ATU should be used.

## Clock and Reset Generation

### Clock Generation

The CG1-RADIO is clocked by a single, 33 MHz signal. This master clock controls the entire timing of the i960<sup>®</sup> RP. The main clock input is fed by one of two possible sources, chosen by the 2x1 clock selection jumper JCLK near the J1 connector on the CG1-RADIO:

#### Clock Selection Jumper JCLK Setting Options

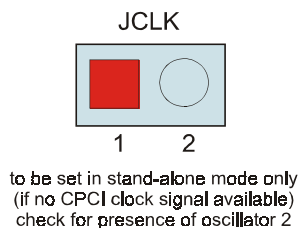
Clock Source	JCLK
<i>CompactPCI</i> <sup>®</sup> Bus Clock Signal (J1 Pin D6)	removed
33 MHz Oscillator on the CG1-RADIO	set

Normally the CG1-RADIO will be integrated in a *CompactPCI*<sup>®</sup> rack with a system controller and possibly other boards. In this case the bus clock signal must be used as clock source (JCLK removed!).

To support a single stand-alone operation without system controller the CG1-RADIO provides an optional on-board 33 MHz oscillator that generates the necessary clock. When setting the jumper JCLK the oscillators output is connected to the clock input of the board.

Note that in this case the clock signal also occurs on the clock pin of the *CompactPCI*<sup>®</sup> connector J1 (Pin D6). This will lead to clock signal crashing on the bus if more than one board drives the clock.

The clock signal is distributed on the CG1-RADIO via a dedicated clock buffer to provide a low skew, well conditioned signal as required by the PCI specification.



The jumper JCLK is regularly not stuffed on the CG1-RADIO, resulting in a CPCI bus clocking of the local CPU.

## Power-On and Manual Reset

There are several reasons which trigger a reset on the CG1-RADIO:

- Power-On (switching on the power supply)
- $V_{cc5}$  drops below 4.65V (power failed)
- $V_{cc3}$  drops below 3.0V (power failed)
- Pushing the RESET Push Button in the front panel
- Triggering the *CompactPCI*® reset signal (J1 Pin C5, JCNF(4) on)
- Reaching time out of the hardware watchdog
- Software reset caused by the i960®RP processor

The first 6 sources will reset all devices on the CG1-RADIO to a known state. An integrated power supervisor generates a clean reset signal with a minimum length of 140 ms even if the voltages haven't stabilized at power-on. The signal is fed to the i960®RP, the Flash EEPROMs and the serial controllers 16C550. The processor can reset all the 16C550s by triggering the local bus reset signal in the Extended Bridge Control Register (EBCR, bit 5).

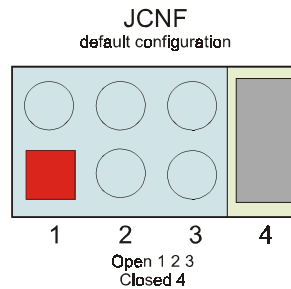
## Hardware Watchdog

The CG1-RADIO is equipped with a hardware watchdog. The watchdog is disabled after a hardware reset. It is activated by toggling the general purpose output OUT1# of port 1's UART. This is done by changing bit 2 in the Modem Control Register MCR of the UART (see section *Serial Controller 16C550* for details of the UART's registers).

If the processor once touched MCR(2), the watchdog is armed and must be triggered at least every 1000 ms. A hardware reset will occur after a maximum time of 1.6 sec after the last watchdog trigger pulse.

## i960<sup>®</sup>RP Initialization Modes

The behavior of the i960<sup>®</sup>RP after reset is controlled by the configuration selection jumper field JCNF. The processor supports four initialization modes 0 to 3, where mode 1 makes no sense on the CG1-RADIO.



### Configuration Jumper Field JCNF Initialization Mode Setting Options

Initialization Mode	JCNF 1	JCNF 2	CompactPCI <sup>®</sup> Interface	i960RP Core Processor
Mode 0	set	set	accepts transactions	held in reset
Mode 1 <sup>1)</sup>	set	removed	retries all config. transactions	held in reset
Mode 2	removed	set	accepts transactions	initializes
Mode 3 (Default)	removed	removed	retries all config. transactions	initializes

<sup>1)</sup> Not useful on the CG1-RADIO

Mode 0 allows a host processor to configure the i960<sup>®</sup>RP peripherals while the i960 core processor is held in reset. The host processor configures the PCI-to-PCI bridge by assigning bus numbers, allocating PCI address space, and assigning IRQ numbers. The memory controller and ATU can also be initialized by the host processor. Program code for the i960 core processor may be downloaded into local DRAM or Flash EEPROM by the host processor. The host processor then clears the i960 reset signal by clearing the Core Processor Reset bit in the Extended Bridge Control Register (EBCR, bit 1). This deasserts the internal reset signal on the i960 core processor and the processor begins its initialization process.

Mode 2 allows configuration cycles on the PCI-to-PCI bridge at any time and allows the i960 core processor to initialize after reset. Mode 2 allows each unit of the i960<sup>®</sup>RP to be initialized in its own manner. Be aware that race conditions may exist between i960 core operation after reset and host processor PCI configuration.

Mode 3 allows the i960 core processor to initialize and control the initialization process before the host processor is allowed to configure the i960<sup>®</sup>RP peripherals. During this time, the CompactPCI<sup>®</sup> interface signals a Retry on all configuration cycles it receives until the i960 core processor clears the Configuration Cycle Disable bit in the EBCR. This is the JCNF default configuration when using the CG1-RADIO with EKF drivers.

The 3<sup>rd</sup> jumper of JCNF exists to enable or disable the i960<sup>®</sup> RP's build-in self test (BIST). If enabled the processor tries to check all its internal units. If the check failed the processor asserts a signal that lights the red on-board LED CPU FAIL and core execution stops. Because BIST needs about 414000 CPU cycles it may be necessary to disable it when the restart time needs to be minimized.

#### Configuration Jumper Field JCNF BIST Setting Options

JCNF 3	Processor BIST
removed (default)	enabled
set	disabled

Jumper 4 of JCNF is used to forward the reset signal from the *CompactPCI*<sup>®</sup> bus to the local CPU and the other local devices on the board.

#### Configuration Jumper Field JCNF CPCI Reset Setting Options

JCNF 4	CPCI Reset
removed	ignored
set (default)	forwarded to the board

It is a good idea to remove JCNF 4 when the BIOS of the main CPU board within the *CompactPCI*<sup>®</sup> does not recognize the CG1-RADIO after system reset.

## Interrupts

The i960<sup>®</sup>RP provides an on-chip programmable interrupt controller that allows a flexible, priority level based reaction to internal and external events. The processor uses interrupt vector numbers to enter the interrupt service routine (ISR). This mechanism leads to fast reaction and low interrupt latency. To optimize interrupt performance the vectors can be hold in the i960<sup>®</sup>RP internal RAM and the ISR can be frozen in the instruction cache. See the i960<sup>®</sup>RP manual for details.

Internal interrupt events have their origin by the different units within the i960<sup>®</sup>RP like the I<sup>2</sup>C unit, the messaging unit etc. External requests are fed to the processor via 2 maskable (XINT0#...XINT1#) and one non-maskable (NMI#) interrupt inputs. Four bits within the PCI interrupt routing select register (PIRSR) decide for each XINT#-pin whether the interrupt is lead to the i960 core or to the *CompactPCI*<sup>®</sup> interface.

The CG1-RADIO owns the following peripheral interrupt devices:

- the serial controllers via XINT0# or XINT0# - XINT1# depending on interrupt mode in use
- the NMI push button (optional, normally not stuffed) via NMI# (non-maskable!)

For a description of the serial controller interrupts refer to the corresponding chapter.

The optional NMI push button is located at the backside of the RESET push button. Since no space was available in the front panel the button is directed toward the board center.

The NMI push button is a nice tool when debugging software on the CG1-RADIO. A debugger can take over control of a running program when pushing the NMI push button. Because this interrupt can not be masked by a program, getting program control is always possible. The interrupt request of the NMI button is active while the button is pushed. It can be identified by checking the NMI interrupt status register (NISR, bit 8). Contact EKF when you need a CG1-RADIO board with NMI button stuffed.

## Local Memory Devices

### Flash EEPROM

The CG1-RADIO is equipped with on-board programmable Flash EEPROM devices. The data bus width to these devices is 32-bit allowing the i960<sup>®</sup>RP to execute program code from Flash in full speed. Therefore it is not necessary to copy the code into DRAM. The Flash devices are connected to the memory bank 0 of the i960<sup>®</sup>RP Memory Controller. They are readable and especially writeable any time with no need to enable the programming voltage. Caution is given when the processor itself tries to program the Flash devices while executing code out of the Flash. This will lead the local CPU to hang up. To program the Flash devices use one of the following alternates:

1. Programming by i960<sup>®</sup>RP core processor: Copy the program data and the Flash programming algorithm code to DRAM. Run the programming code from DRAM. Return to the calling function or restart the code loaded into the Flash devices.
2. Programming via *CompactPCI*<sup>®</sup> interface: Reset the CG1-RADIO with jumper field JCNF set to initialization mode 0. Alternatively the i960<sup>®</sup>RP core processor could be halted by executing the HALT instruction. Program the Flash devices via the primary ATU. Restart the processor.

A utility which allows to program the Flash across the CPCI interface without prior modifying JCNF is part of the drivers package available from EKF (observe the attached Readme information file to step through the programming procedure).

Depending on the version of the CG1-RADIO there are different types of Flash devices in use:

- 28F016SV Intel/Sharp
- 28F160S5 Intel/Sharp

These devices distinguish in access times and programming algorithms. Programming tools (currently running on LINUX or WinXX) are offered by EKF and are available on request. The following table shows the necessary initializations in the read and write wait state registers (MBRWS0, MBWWS0) of the i960<sup>®</sup>RP memory controller dependent on the devices in use. All timing parameters are based on a clock frequency of 33.33 MHz (corresponding to 30 ns cycle time):

Flash Device Read And Write Wait State Settings

Flash Device	Read		Write	
	Access [ns]	MBRWS0	Access [ns]	MBWWS0
28F016SV	70	0x00000220	70	0x00000221
28F160S5	70	0x00000220	70	0x00000220

## Dynamic Random Access Memory (DRAM)

The CG1-RADIO offers a working memory space of 4 Mbyte. The memory is organized as a bank of non-interleaved DRAM, 4 Mbyte in size. The data path width is 32-bit without parity. Similar to the Flash EEPROMs different types of DRAM devices are in use. Possible types are

- Fast Page Mode (FPM) DRAMs
- Extended Data Out (EDO) DRAMs

with an access time of at least 70 ns. The following table shows typical values to program to the i960<sup>®</sup>RP memory controller to setup the DRAM interface. All timing parameters are based on a clock frequency of 33.33 MHz (corresponding to 30 ns cycle time):

DRAM Initialization Parameters

Name	Register	Value	Description
DRWS	DRAM Bank Read Wait State	0x00000000	RAS-to-CAS delay 1.5 cycles, CAS pulse width 1.5 cycles, no additional recovery wait states
DWWS	DRAM Bank Write Wait State	0x00000000	RAS-to-CAS delay 1.5 cycles, CAS pulse width 1.5 cycles, no additional recovery wait states
DRIR	DRAM Refresh Interval	0x00010204	Refresh enabled, 15.625 $\mu$ s refresh interval
DPER	DRAM Parity Enable	0x00000000	DRAM parity disabled
DBCR	DRAM Bank Control	0x0000000D 0x0000004D	High-current drives disabled, DRAM bank enables, Fast Page Mode (FPM), 2 banks or Extended Data Out (EDO), 2 banks

## I<sup>2</sup>C Interface

The i960<sup>®</sup>RP supports a master and slave interface to the popular I<sup>2</sup>C (Inter-Integrated Circuit) bus. This simple, two wire serial bus allows an easy connection to other I<sup>2</sup>C devices. Transfer rates of up to 400 Kbit/s are possible. It could be programmed via the I<sup>2</sup>C unit registers of the i960<sup>®</sup>RP.

An I<sup>2</sup>C message consists of a device addressing byte and additional data bytes. The device address byte also contains the information whether the following operations are read or write transfers. If the address of an I<sup>2</sup>C slave device on the bus matches the device address byte sent by a master, the slave acknowledges the transfer.

General I<sup>2</sup>C Addressing Byte Format

A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	R/W
MSB							LSB

On write operations (R/W=0) the master may send then further data bytes to the slave until the master generates a stop condition. Each byte transferred is acknowledged by the recipient. Read operations are working in the same way except that R/W=1 and that the data flow is reversed.

### Serial EEPROM 24C32

The CG1-RADIO offers a serial EEPROM 24C32 with a capacity of 4 Kbytes. This device can be used e.g. to permanently store important parameters that should be non volatile even if the power disappears. It is accessible as slave device via the I<sup>2</sup>C bus. Write accesses to the memory array of the serial EEPROM are possible any time because the hardware write protection feature of the 24C32 is not enabled on CG1-RADIO.

Serial EEPROM 24C32 Addressing Byte Format

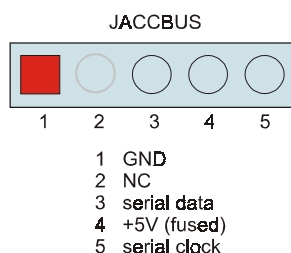
1	0	1	0	0	0	0	R/W
MSB				A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	LSB

The above figure shows the I<sup>2</sup>C bus device addressing byte that must be written to the serial EEPROM in order to read (R/W=1: DeviceAddr=0xA1) or write (R/W=0: DeviceAddr=0xA0) data from or to it (the 3 external address lines A<sub>2-0</sub> offered by the 24C32 are hard-wired to GND on the CG1-RADIO). Read and write accesses with the I<sup>2</sup>C bus maximum speed of 400 Kbit/s are supported by the device.

## ACCESS.bus Interface

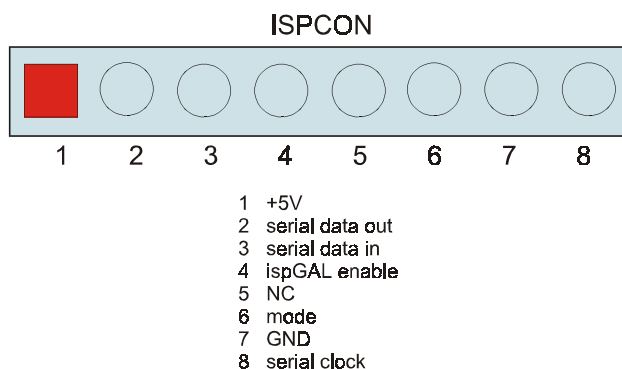
To make it easy to connect external I<sup>2</sup>C devices to the CG1-RADIO the board offers an ACCESS.bus interface via the 4-pin connector **JACCBUS**. The ACCESS.bus is similar to the System Management Bus (SMBus) based on the I<sup>2</sup>C bus. Both standards are compatible to the I<sup>2</sup>C bus with exception of a few electrically (e.g. max. load capacity) and mechanical (e.g. ACCESS.bus defines a connector, I<sup>2</sup>C does not) specifications.

The ACCESS.bus interface on the CG1-RADIO supports up to 126 devices (7-bit device addresses minus the broadcast address and the on-board serial EEPROM) over a total cable length of 8 m with a maximum data rate of 100 Kbit/s. Each device may use its own data rate. The cable consists of two shielded pairs: a Ground/+5V pair and a clock/data pair.



## PLD Programming Header

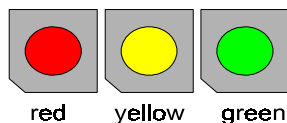
Most of the boards glue logic is contained in a programmable logic chip (ispGAL). Low level address decoding, interrupt routing and watchdog/reset behaviour is controlled by firmware. The ispGAL is programmable on-board, by using the ISPCON interface connector:



Note: The ISPCON is not normally stuffed.

## CPU Diagnostics Display

There are three on-board LEDs (hence visible with an open enclosure only) on the CG1-RADIO indicating the current state of the processor. This row of LEDs is located near the Lithium cell:



CPU Diagnostics  
Display

### Diagnostics Display Information

LED	on	off
LED 'CPU Fail' (red) core state	build-in self test failed, or local bus confidence test failed, or processor held in reset state: core execution stopped	both build-in self test and local bus confidence test passed: core is in executing mode
LED 'UART Acc.' (yellow)	access to one of the serial controllers	no access to any of the serial controllers
LED 'LOCAL Acc.' (green)	access to local DRAM, Flash or UARTs	no access to any local device

## JTAG Test Port

The JTAG port is a dual row, 10-pos. header. It is normally not stuffed, since the JTAG signals are routed to the CPCI connector J1 in parallel.

	JTAG		
TRST#	1	2	GND
TDO	3	4	GND
TDI	5	6	GND
TMS	7	8	GND
TCK	9	10	GND

## Additional Documentation

A detailed description including the programming of the i960<sup>®</sup>RP processor could be found in the documentation listed below. Electronic information can be obtained from

<http://developers.intel.com>

### i960<sup>®</sup>RP Related Documentation

Document Title	Order Number
<i>i960<sup>®</sup>Rx I/O Microprocessor Developer's Manual</i>	Intel Order # 272736
<i>i960<sup>®</sup>Rx I/O Processor Specification Update</i>	Intel Order # 272918
<i>i960<sup>®</sup>RP/RD I/O Processor at 3.3 Volts data sheet</i>	Intel Order # 273001
<i>i960<sup>®</sup>Jx Microprocessor User's Guide</i>	Intel Order # 272483

## Serial Interfaces

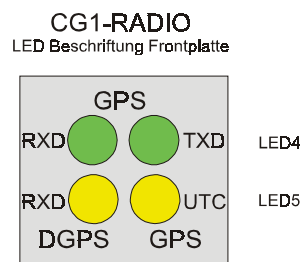
### General Information

The CG1-RADIO is provided with two serial interfaces. The first one is directly connected to the NMEA (primary port) of the Jupiter GPS receiver. Commands and data are passed bidirectionally across this interface, either ASCII coded using the NMEA protocol (by default), or using the Rockwell/Conexant binary (proprietary) protocol. This port normally operates at 4800bps, no parity, 8 data bits, one stop bit, and is not available for external usage.

The second serial port is available by the front panel connector SP2, configured as RS-232E interface. It is intended mainly to receive RTCM DGPS data to sharpen GPS positioning information. A tap is established leading to the auxiliary serial interface on the Jupiter module. This port normally operates at 9600bps, no parity, 8 data bits, one stop bit, when used as DGPS input. The Ring Indicator (RI) signal pin can be used as the power source to the external DGPS receiver (requires jumper JWZ closed).

If there is no need for an external DGPS receiver (due to deactivated GPS SA, or when using GPS timing information only), the second serial port SP2 can be used as general purpose serial interface, like any PC style COM port. The connector SP2 and the corresponding jumper JWZ are described in detail later on in this document.

There are indicator LEDs mounted in the front panel to signal both RXD and TXD of the first (internal) serial interface, and RXD only of the second serial interface.



Mounted on-board (hence visible with an open enclosure only), three other LEDs are used to signal debugging information to the system integrator:

LED 'UART Acc.' (yellow) located near the Lithium cell	lightens whenever signal CE1# is active, which is an output directly from the i960 processor, and is fed to an input of the ispGAL for further address decoding.
LED 'CS UART' (yellow) located near the DRAM	lightens whenever either of the two UART chip select lines is activated, or lightens on other events when programmed accordingly by ispGAL firmware
LED 'IRQ UART' (red) located near the DRAM	lightens whenever an interrupt from either of the UARTs is pending (waiting for service routine), or lightens on other events when programmed accordingly by ispGAL firmware

## Serial Controller 16C550

The serial interfaces are based on the well known Asynchronous Communication Element (ACE) 16C550. These UARTs are clocked with 14.7456 MHz leading to transfer rates of up to 921.6 KBaud.

The next table shows the transmission bit rates, the value of the UART's divisor latch register (iDiv) and the resulting baud rate errors in dependency of the clock in use:

UART Data Transmission Bit-Rates

Clock	Baud	Divisor	iDiv	Error
14745600	75	12288.0	12288	0.00%
14745600	110	8378.2	8378	0.00%
14745600	135	6826.7	6827	0.00%
14745600	150	6144.0	6144	0.00%
14745600	300	3072.0	3072	0.00%
14745600	600	1536.0	1536	0.00%
14745600	1200	768.0	768	0.00%
14745600	1800	512.0	512	0.00%
14745600	2400	384.0	384	0.00%
14745600	4800	192.0	192	0.00%
14745600	7200	128.0	128	0.00%
14745600	9600	96.0	96	0.00%
14745600	14400	64.0	64	0.00%
14745600	19200	48.0	48	0.00%
14745600	38400	24.0	24	0.00%
14745600	56000	16.5	16	-2.78%
14745600	57600	16.0	16	0.00%
14745600	115200	8.0	8	0.00%
14745600	128000	7.2	7	-2.78%
14745600	230400	4	4	0.00%
14745600	460800	2	2	0.00%
14745600	921600	1	1	0.00%

The UARTs are connected to bank 1 of the i960<sup>®</sup> RP's memory controller. The following table shows the addressing of the registers of the 1<sup>st</sup> UART relative to its base address:

UART (16C550) Register Offset Definitions

Base Address Offset	Read Access	Write Access
0x00	Receiver Buffer Register (RBR)	Transmitter Holding Register (THR)
0x04	Interrupt Enable Register (IER)	Interrupt Enable Register (IER)
0x08	Interrupt Ident. Register (IIR)	FIFO Control Register (FCR)
0x0C	Line Control Register (LCR)	Line Control Register (LCR)
0x10	Modem Control Register (MCR)	Modem Control Register (MCR)
0x14	Line Status Register (LSR)	not allowed
0x18	Modem Status Register (MSR)	ignored
0x1C	Scratch Register (SCR)	Scratch Register (SCR)

The 1<sup>st</sup> register of the UART of the 2<sup>nd</sup> port starts at relative address 0x20

UART (16C550) Port Offset Definitions

Port Number	1	2
Base Address Offset	0x00	0x20

In order to get a proper function of the UARTs, the following values should be programmed to the wait state registers of memory bank 1. Burst accesses to the UARTs are not allowed.

UART (16C550) Read And Write Wait State Settings

MBRWS1	MBWWS1
0x00000302	0x00000302

The UARTs are able to request i960<sup>®</sup>RP core interrupts. On the CG1-RADIO are two interrupt modes available:

- Collected Interrupt Mode: The request lines of both UARTs are pulled together to the interrupt input XINT0# of the processor (default mode after reset).
- Distributed Interrupt Mode: The request lines of the UARTs are fed to XINT0# - XINT1# of the processor.

The interrupt mode is chosen by the general purpose output OUT2# of the 1<sup>st</sup> UART. This port can be switched by accessing bit 3 of the Modem Control Register MCR:

#### Interrupt Mode Selection

Interrupt Mode	MCR(3)
Collected Interrupt Mode (default after reset)	0
Distributed Interrupt Mode	1

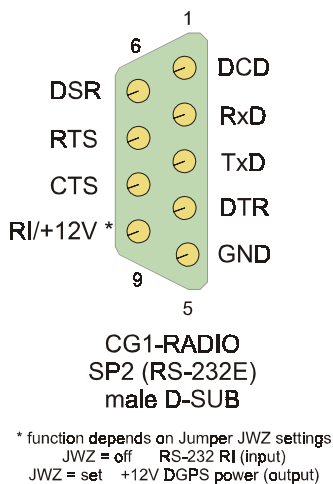
#### Distributed Interrupt Mode Request Pin Table

Port Number	1	2	3	4	5	6	7	8
Port Number	9	10	11	12	13	14	15	16
Interrupt Request Pin	XINT0#	XINT1#	XINT2#	XINT3#	XINT4#	XINT5#	XINT6#	XINT7#

An IRQ can be identified by checking the IIR of the UART in the interrupt service routine. The request is released by accessing the corresponding register that caused the interrupt (e.g. reading an incoming character from the RBR). See UART data sheets and i960<sup>®</sup>RP manual for detailed description of interrupt programming.

Connector SP2, Jumper JWZ

The illustration below shows the pin assignment of the connector SP2 (front view to the connector). Signal directions are seen from the view of the CG1-RADIO, e.g. RXD (SP2, pin 2) is an input to the CG1-RADIO. It is assumed, that jumper JWZ is open:



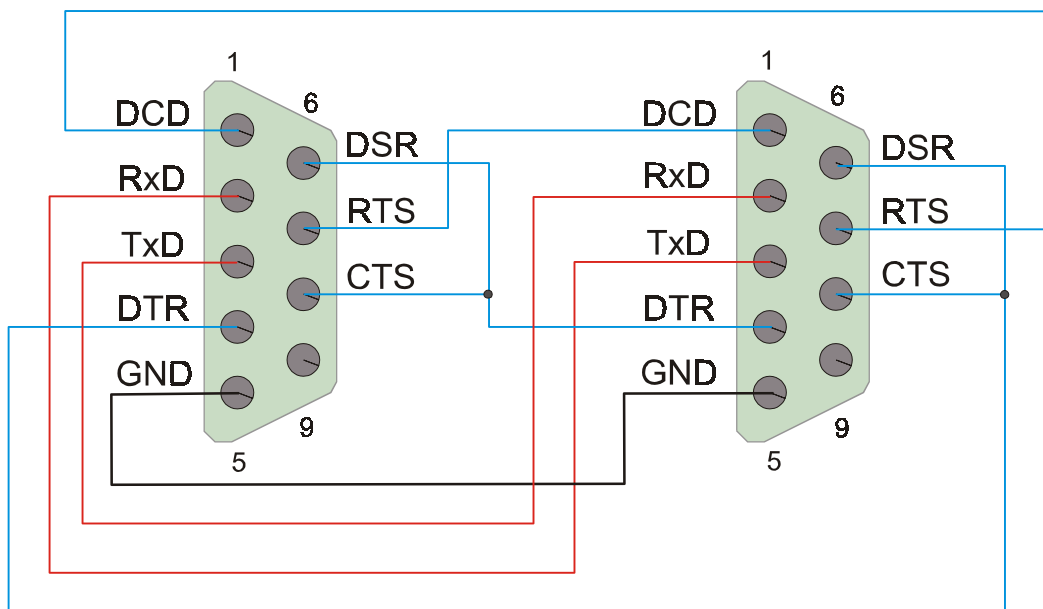
Male D-Sub 9 Connector (PC compatible)

SP2 (RS-232E)		
	1	DCD
DSR	6	
	2	RXD
RTS	7	
	3	TXD
CTS	8	
	4	DTR
RI	9	
	5	GND

The signal RXD (typically data from external DGPS receiver) can be observed from an indicator LED mounted in the front panel of the CG1-RADIO.

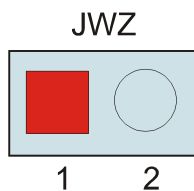
The following figure shows the wiring scheme of a standard RS-232 link cable usually in use to connect a port of the CG1-RADIO with another RS-232 port, e.g. a COM port of a PC:

### Link Cable RS-232 for interconnection between CG1-RADIO serial port (SP2) and PC COM port



connectors: shielded female D-SUB 9  
complete cable assembly available  
EKF part no. 280.7.201

Some DGPS receivers require a +12V power source on the pin 9 of the D-SUB connector, which is defined as signal RI (Ring Indicator) for modem operation. The jumper JWZ must be closed for DGPS +12V, and open for RI signal:

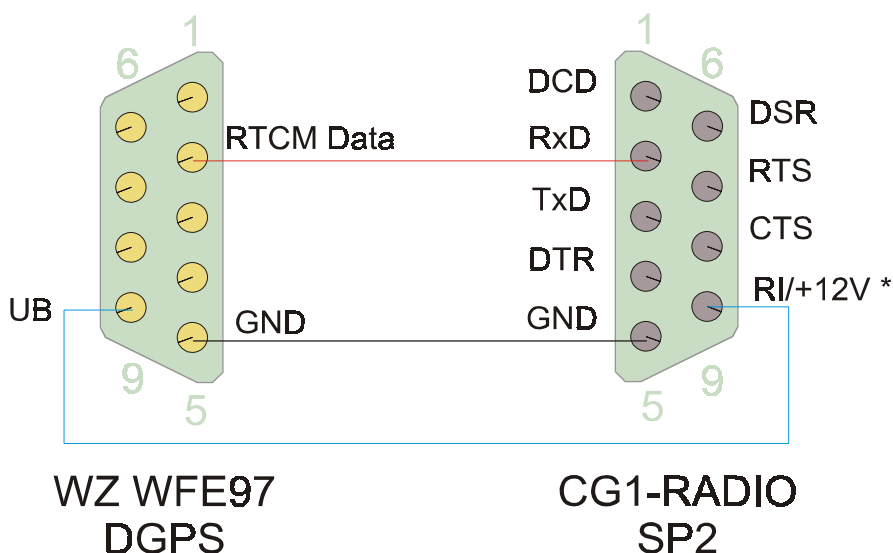


JWZ determines function of SP2 pin 9  
jumper off = RS-232 RI input (default)  
jumper set = +12V/50mA power output

To establish a connection between the serial port SP2 and the external DGPS receiver, a three wire cable should be used as shown in the diagram below:

### Connection Cable RS-232

for interconnection between  
CG1 serial port (SP2) and  
WZ WFE97 DGPS Receiver



connectors shielded D-SUB 9  
CG1-RADIO: female connector  
WZ WFE97 DGPS: male connector  
cable is included with DGPS receiver

\* function depends on JWZ jumper settings  
jumper must be set in order to provide  
WZ DGPS receiver with +12V power

## CompactPCI® Interface

The CG1-RADIO offers a *CompactPCI*® interface complying to the *CompactPCI*® Specification Revision 2.1. *CompactPCI*® is an industrial implementation of the familiar *Peripheral Component Interconnect* (PCI) bus. It combines the well known electrical features of PCI with the more robust mechanical 19 inch rack mounting technology. The interface supports 64-bit address and 32-bit data transfers. It is designed for a clock frequency of 33 MHz with a transfer rate of up to 132 Mbyte/s.

## PCI Devices

The *CompactPCI*® interface is realized by the i960® RP processor. It consists of two PCI functions, thus it is a multi-function PCI device. The first function (PCI function 0) is the PCI-to-PCI bridge unit which creates a data path between the primary (the *CompactPCI*®) and the secondary interface (not used on CG1-RADIO). PCI function 1 is the primary Address Translation Unit (ATU). This unit allows high-speed accesses from the *CompactPCI*® interface to the local bus devices like Flash EEPROM or DRAM. Normally a BIOS running on a host system detects these PCI devices at boot time.

## Address Translation Unit (ATU)

The Address Translation Unit (ATU) provides an interface between the *CompactPCI*® bus and the i960 local bus. It consists of two parts: the primary ATU for accesses from *CompactPCI*® and the secondary ATU for accesses from the secondary PCI bus (not used on the CG1-RADIO). Data transfers initiated by any PCI bus master to a local bus device are called *inbound* transactions. If the i960 core starts a data access to any PCI bus slave, this is called an *outbound* transfer.

The ATU fulfils both address filtering and address translation. For inbound transactions the ATU uses three registers:

- Inbound ATU Base Register
- Inbound ATU Limit Register
- Inbound ATU Translate Value Register

A PCI address is detected as an inbound transaction by the ATU if

$$(\text{PCI\_Address} \& \text{Limit\_Register}) == \text{Base\_Register}.$$

The incoming 32-bit `PCI_Address` is bitwise ANDed with the `Limit_Register`. When the result matches the `Base_Register`, the `PCI_Address` is detected as being within the inbound translation window. This opens a PCI address window from (`Base_Register`) to (`Base_Register + Limit_Register`). Once the transaction is claimed, the address must be translated from a 32-bit PCI address to a 32-bit local address. For that, the incoming `PCI_Address` is first bitwise ANDed with the bitwise inverse of the `Limit_Register`. This result is bitwise ORed with the `ATU Translate_Value_Register`. The result is the 32-bit local address:

$$\text{Local\_Address} = (\text{PCI\_Address} \& (\sim \text{Limit\_Register})) \mid \text{Translate\_Value\_Register}$$

In addition the ATU provides address detection and translation for i960 core processor-initiated cycles targeted to one of the PCI buses. The ATU supports two different translation modes:

- Address Translation Windows
- Direct Addressing Window

The address translation windows are located from 0x8000 0000 to 0x9001 FFFF within the 32-bit local address space of i960 processor. This range consists of two 128 Mbyte memory windows and two 64 Kbyte I/O windows for the primary and secondary ATU respectively. Each memory window is divided into two areas, 64 Mbyte for 32-bit PCI address cycles and 64 Mbyte for PCI double address cycles (DAC). The type of the PCI transfer is dependent from the area that is hit within the address translation window by the i960 core.

The translation mechanism used is very similar to the algorithm for the inbound transactions described above. For memory and DAC accesses it is

$$\text{PCI\_Address} = (\text{Local\_Address} \& \text{0x03FF FFFF}) | \text{Memory\_Window\_Value\_Register}$$

I/O transactions are translated by

$$\text{PCI\_Address} = (\text{Local\_Address} \& \text{0x0000 FFFF}) | \text{I/O\_Window\_Value\_Register}$$

In addition the i960<sup>®</sup>RP provides a direct addressing scheme. This method of outbound PCI transactions is limited to memory transfers and works within the local address range from 0x0000 2000 to 0x7FFF FFFF only. If enabled any access to these locations are forwarded to the PCI bus. Which of the PCI buses are used will be decided by a bit in the ATU control register ATUCR. This register also contains the direct addressing enable bit.

As every PCI device the ATU implements its own configuration space. This space is 256 bytes in size, whereas the first 64 bytes must adhere to a predefined header format. The ATU is programmed on the *CompactPCI*<sup>®</sup> interface via type 0 configuration commands to PCI function number one. Besides the i960 core processor can access the configuration space via memory mapped registers at local address 0x1200. Some of the read-only registers can also be written by the i960. The following table shows the configuration header according the *PCI Local Bus Specification*, revision 2.1:

## Address Translation Unit Configuration Header Format

Address Translation Unit Configuration Header				Address Offset
ATU Device ID		ATU Vendor ID		0x00
ATU Primary Status		ATU Primary Command		0x04
ATU Class Code			ATU Revision ID	0x08
BIST	Header Type	Latency Timer	Cacheline Size	0x0C
Primary Inbound ATU Base Address				0x10
Reserved				0x14
				0x18
				0x1C
				0x20
				0x24
				0x28
ATU Subsystem ID		ATU Subsystem Vendor ID		0x2C
Expansion ROM Base Address				0x30
Reserved				0x34
				0x38
Max. Latency	Minimum Grant	Interrupt Pin	Interrupt Line	0x3C

The next table shows the i960<sup>®</sup>RP specific registers of the ATU configuration space.

ATU Extended PCI Configuration Header Format

ATU Extended PCI Configuration Register Space		Address Offset
Primary Inbound ATU Limit Register PIALR		0x40
Primary Inbound ATU Translate Value Register PIATVR		0x44
Secondary Inbound ATU Base Address Register SIABAR		0x48
Secondary Inbound ATU Limit Register SIALR		0x4C
Secondary Inbound ATU Translate Value Register SIATVR		0x50
Primary Outbound Memory Window Value Register POMWVR		0x54
Reserved		0x58
Primary Outbound I/O Window Value Register POIOWVR		0x5C
Primary Outbound DAC Window Value Register PODWVR		0x60
Primary Outbound Upper 64-bit DAC Register POUDR		0x64
Secondary Outbound Memory Window Value Register SOMWVR		0x68
Secondary Outbound I/O Window Value Register SOIOWVR		0x6C
Reserved		0x70
Expansion ROM Base Address Register ERBAR		0x74
Expansion ROM Translate Value Register ERTVR		0x78
Reserved		0x7C
		0x80
		0x84
ATU Configuration Register ATUCR		0x88
Reserved		0x8C
Primary ATU Interrupt Status Register PATUISR		0x90
Secondary ATU Interrupt Status Register SATUISR		0x94
Secondary ATU Status Register	Secondary ATU Command Register	0x98
Secondary Outbound DAC Window Value Register SODWVR		0x9C
Secondary Outbound Upper 64-bit DAC Register SOUDR		0xA0
Primary Outbound Configuration Cycle Address Register POCCAR		0xA4
Secondary Outbound Configuration Cycle Address Register SOCCAR		0xA8
Primary Outbound Configuration Cycle Data Register POCCDR		0xAC
Secondary Outbound Configuration Cycle Data Register SOCCDR		0xB0
Reserved		0xB4 - 0xFF

## System Connector J1

The *CompactPCI*<sup>®</sup> specification defines the usage of shielded, 2 mm-pitch, 5-row connectors on *CompactPCI*<sup>®</sup> boards according to IEC 917 and IEC 1076-4-101. The 32-bit PCI interface is implemented via the J1 connector, while the 64-bit option requires the connector J2. Since the CG1-RADIO has a 32-bit *CompactPCI*<sup>®</sup> interface, the J2 connector is not necessary and thus not mounted.

The J1 connector also defines the supported signaling voltage ( $V_{VO}$ ). A coding key in this connector is used to distinguish boards with  $V_{VO}=3.3V$  (cadmium yellow key),  $V_{VO}=5V$  (brilliant blue key) or both (no key). The CG1-RADIO is suitable for  $V_{VO}=5V$  only and equipped with a blue coding key.

CAUTION: Do not use the CG1-RADIO within a 3.3V *CompactPCI*<sup>®</sup> system.

## CompactPCI J1

#J1	A	B	C	D	E
25	5V	<i>REQ64#</i>	<i>ENUM#</i>	3.3V	5V
24	AD1	5V	VI/O	AD0	<i>ACK64#</i>
23	3.3V	AD4	AD3	5V	AD2
22	AD7	GND	3.3V	AD6	AD5
21	3.3V	AD9	AD8	M66EN (GND)	C/BE0#
20	AD12	GND	VI/O	AD11	AD10
19	3.3V	AD15	AD14	GND	AD13
18	SERR#	GND	3.3V	PAR	C/BE1#
17	3.3V	<i>IPMB SCL</i>	<i>IPMB SDA</i>	GND	PERR#
16	DEVSEL#	GND	VI/O	STOP#	LOCK#
15	3.3V	FRAME#	IRDY#	GND	TRDY#
14					
13			5V KEY		
12					
11	AD18	AD17	AD16	GND	C/BE2#
10	AD21	GND	3.3V	AD20	AD19
9	C/BE3#	IDSEL	AD23	GND	AD22
8	AD26	GND	VI/O	AD25	AD24
7	AD30	AD29	AD28	GND	AD27
6	REQ#	GND	3.3V	CLK	AD31
5	<i>BRSVP1A5</i>	<i>BRSVP1B5</i>	RST#	GND	GNT#
4	<i>BRSVP1A4</i>	GND	VI/O	<i>INTP</i>	<i>INTS</i>
3	INTA#	INTB#	INTC#	5V	INTD#
2	TCK	5V	TMS	TDO	TDI
1	5V	-12V	TRST#	+12V	5V

*pin positions printed italic/gray: not connected*

## Literature

Theme	Document Title	Origin
CompactPCI Specification	CompactPCI Specification, PICMG 2.0 R3.0, Oct. 1, 1999	PICMG ( <a href="http://www.picmg.org">http://www.picmg.org</a> )
PCI	PCI Hardware and Software Architecture & Design, Solari/Willse, 4th Edition, Annabooks	Annabooks ( <a href="http://www.annabooks.com">http://www.annabooks.com</a> )
Metric Connectors	IEC 1076-4-101 Application Literature from ERNI, AMP, FCI	Beuth Verlag, Berlin ILI Index House, GB SL57EU Ascot Berkshire
2.54mm Shrouded Headers	DIN 41651	Beuth Verlag, Berlin

## Ordering Information

Alias	Ordering No.	Short Description
RADIO	CG1-1-RADIO	3U CompactPCI hostadapter, 12-channel GPS receiver subsystem with i960RP CPU/bridge, 4MB Flash, 4MB DRAM, MON960
	CR9-1-ADAPT	Front panel expansion kit 3U → 6U
	940.80.30149.1	GPS antenna, active +5V, SMB connector, 5m cable length
	940.80.90100.1	External DGPS LW receiver box, including ALF license (Accurate Positioning by Low Frequency, transmitter Mainflingen/Frankfurt, receiver radius about 650km), not required while deactivation of GPS SA function

EKF Elektronik GmbH  
Philipp-Reis-Str. 4  
D-59065 HAMM  
(Germany)



Internet <http://www.ekf.de>  
Fax. +49 (0)2381/6890-90  
Tel. +49 (0)2381/6890-0  
E-Mail [info@ekf.de](mailto:info@ekf.de)